

ABSTRACT OF THE DISCLOSURE

A novel bi-level DRAM architecture is described which achieves significant reductions in die size while maintaining the noise performance of traditional folded architectures. Die size reduction results primarily by building the memory arrays with $6F^2$ or smaller memory cells in a type of cross-point memory cell layout. The memory arrays utilize stacked digitlines and vertical digitline twisting to achieve folded architecture operation and noise performance.

N:\2269\3351.8\cont.pat.app.revised.clean.doc